P.D. 2000
P. 1186-1193

XP-002243765

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 8, AUGUST 2000

Impact of Extrinsic and Intrinsic Parameter Fluctuations on CMOS Circuit Performance

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Abstract—**The yield of CMOS logic circuits satisfying a specific high performance requirement is demonstrated to be significantly influenced by the magnitude of critical-path delay deviations due to both extrinsic and intrinsic parameter fluctuations. To evaluate the impact of these parameter fluctuations, a static CMOS critical-path delay distribution is calculated from rigorously derived device and circuit models that enable projections for future technology generations. Two possible options are explored to attain a desired yield: 1) reduce performance by operating at a lower clock frequency; and 2) increase the supply voltage and, consequently, power dissipation, to satisfy the nominal critical-path delay. For the 50-nm technology generation, the delay and power dissipation increases are 12%–29% and 22%–46%, respectively, for extrinsic parameter standard deviations ranging from (a) 5% for effective channel length and 0% for gate oxide thickness and channel doping concentration to (b) 10% for effective channel length and 5% for gate oxide thickness and channel doping concentration. Combining both extrinsic and intrinsic fluctuations, the delay and power dissipation increase to 18%–32% and 31%–53%, respectively, thus demonstrating the significance of including the random dopant placement effect in future CMOS logic designs.**

Index Terms—**Circuit design, CMOS logic circuit performance, critical-path delay variations, gate delay variations, parameter variations, random dopant placement, technology projections.**

I. Introduction

As microelectronic technology continues to advance through reducing the minimum feature size and increasing the number of transistors per chip in accordance with Moore's Law [1], two major circuit design issues are: 1) the nonuniformity of electrical characteristics across the chip; and 2) the increase in power consumption per chip [2]. Extrinsic macroscopic manufacturing process fluctuations and intrinsic microscopic random dopant fluctuations produce deviations in MOSFET drive current, resulting in critical-path delay distributions across the chip. In this paper, the impact of extrinsic and intrinsic fluctuations are quantified by two methods: 1) reduce performance by operating at a lower clock frequency; and 2) increase the supply voltage and, consequently, power dissipation, to satisfy the nominal critical-path delay.

Manuscript received October 15, 1999; revised March 3, 2000. This work was supported by the Semiconductor Research Corporation under Contract SJ-374, the Defense Advanced Research Project Agency under Contract F3361595C1623.

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Publisher Item Identifier S 0018-9200(00)06444-1.

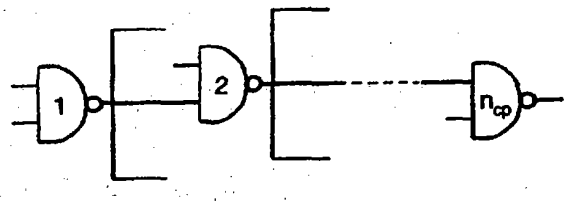

Fig. 1. Critical path model.

Rigorously derived device and circuit models [3] are employed to calculate a critical-path delay distribution for a statistical range of extrinsic fluctuations in effective channel length, doping concentration, and oxide thickness, as well as computed values of intrinsic fluctuations from a stochastic device model [4]. The model equations, derived from fundamental device and circuit analyses, enable projections of extrinsic and intrinsic fluctuations on circuit performance distributions for future technology generations. Depending on the estimated number of critical paths per chip and the desired yield, the permissible increase in delay can be determined. The increase in power dissipation is calculated by shifting the nominal distributions through increasing the supply voltage such that the required nominal critical-path delay is achieved. Therefore, the goal of this paper is to define the impact of extrinsic and intrinsic parameter fluctuations on circuit performance for future generations of technology by evaluating the increases in delay and power dissipation above nominal values that guarantee a specified yield.

The methodology for evaluating the impact of parameter fluctuations on CMOS circuit performance is discussed in Section II along with the results of the extrinsic fluctuations. In Section III, the analytical models used to incorporate the intrinsic fluctuations are presented along with results. In Section IV, the extrinsic and intrinsic parameter fluctuations are combined to analyze the impact on CMOS circuit performance for future generations of technology. Finally, concluding remarks are offered in Section V.

II. Impact of Extrinsic Fluctuations on the Critical Path Delay Distribution

The impact of macroscopic extrinsic parameter fluctuations on circuit performance is quantified by developing and analyzing a critical-path delay distribution using rigorously derived device and circuit models [3], which are advantageous for predicting circuit performance of future technology g nerations. As shown in Fig. 1, the critical path is modeled by a

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number (n_{cp}) of identical two-input static CMOS NAND gates with a fan-out of three [5], where each gate drives an average wiring capacitance calculated from a stochastic interconnect distribution [6]. The static CMOS logic gate was chosen for its low standby power drain, large operating margins, scalability, and flexibility of logic functions [7]. Static and dynamic contributions to power dissipation are considered where the short-circuit power is assumed negligible in high performance/low power designs [3], [8].

To obtain a critical-path delay distribution, the propagation delay distribution of an individual static CMOS NAND gate is first analyzed. The average propagation delay through a two-input NAND gate is modeled by averaging the delay through two-series connected nFET's and the delay through one pFET given as

$$T_{PD,\mathrm{NAND}} = \frac{f_{\mathrm{ineff}} T_{PDn} + T_{PDp}}{2} \tag{1}$$

where f_{ineff} is the effective fan-in factor [9] for series connected MOSFET's and T_{PDn} and T_{PDp} are the nFET and pFET CMOS propagation delay models, respectively, that include the transition (rise or fall) time effect [3].

The extrinsic fluctuations of effective channel length (L), doping concentration (N_A), and oxide thickness (T_{OX}) are assumed to follow uncorrelated Gaussian distributions [10] for the nFET's and pFET's in each gate. Thus, the NAND gate propagation delay distribution density function is calculated from a convolution described as

$$F_{T_{PD,\mathrm{NAND}}} = (f_{\mathrm{ineff}} F_{T_{PDn}}/2) * (F_{T_{PDp}}/2) \tag{2}$$

where $F_{T_{PDn}}$ and $F_{T_{PDp}}$ are the propagation delay distribution density functions for the nFET and pFET respectively. $F_{T_{PDn}}$ and $F_{T_{PDp}}$ are developed by iterating through every parameter combination and its corresponding probability using compact delay models [3] for the nFET and pFET respectively. Since the deviations for each gate in the critical path are equivalent

$$F^1_{T_{PD,\mathrm{NAND}}} = F^2_{T_{PD,\mathrm{NAND}}} = \cdots = F^{n_{cp}}_{T_{PD,\mathrm{NAND}}} \tag{3}$$

the critical-path delay distribution density function is calculated as a Gaussian [11]

$$\begin{aligned} F_{T_{PD,CP}} &= F^1_{T_{PD,\mathrm{NAND}}} * F^2_{T_{PD,\mathrm{NAND}}} * \cdots * F^{n_{cp}}_{T_{PD,\mathrm{NAND}}} \\ &= N(\mu_{T_{PD,CP}}, \sigma_{T_{PD,CP}}). \end{aligned} \tag{4}$$

The mean critical-path delay is calculated as

$$\mu_{T_{PD,CP}} = n_{cp} \mu_{T_{PD,\mathrm{NAND}}} \tag{5}$$

where $\mu_{T_{Pd,\mathrm{NAND}}}$ is the mean NAND gate delay. The critical-path delay standard deviation is computed as

$$\sigma_{T_{PD,CP}} = \sqrt{n_{cp}}\, \sigma_{T_{PD,\mathrm{NAND}}} \tag{6}$$

where $\sigma_{T_{PD,\mathrm{NAND}}}$ is the NAND gate delay standard deviation. Fig. 2 illustrates the separate influences of L, N_A, and T_{OX}, as well as all three parameters combined on the critical-path delay distribution (4)–(6) for a normalized standard deviation of 5% for each parameter. The deviations in effective channel length and oxide thickness are shown to have a more significant contribution to the critical-path delay distribution than variations in doping concentration for a uniform channel doping profile.

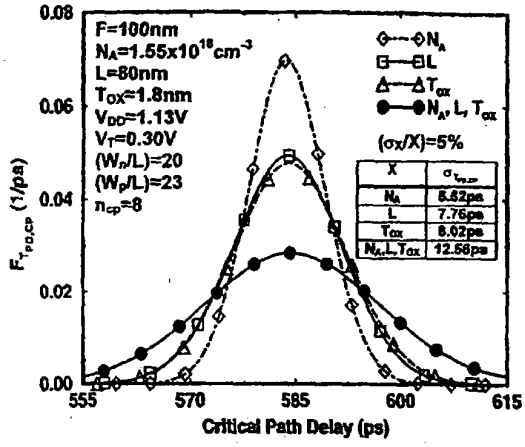

Fig. 2. Critical-path delay distributions for a 5% standard deviation in N_A, L, T_{OX}, and all three combined from (4)–(6).

A chip contains a number of critical paths (N), all of which must satisfy the worst-case delay constraint [10], [12]. Since the fluctuations in each critical path are independent, the probability that all N critical paths meet a specified delay (T), defined in this paper as the yield, is

$$\mathrm{Yield} = \left(\int_0^T F_{T_{PD,CP}}(t)\, dt \right)^N \tag{7}$$

where t is the variable critical-path delay corresponding to parameter fluctuations. As described by (7), yield should be interpreted narrowly as the yield of a testing process in which products are "sorted" according to speed. Typically, this sorting process follows a reliability screening procedure in which products are stressed at elevated temperatures in order to reveal defects, functionality, and reliability problems. Two possible options to achieve a desired yield (7) are: 1) reduce performance by operating at a lower clock frequency; and 2) increase the supply voltage (V_{DD}) and, consequently, power dissipation, to satisfy the nominal critical-path delay. Increasing V_{DD} in the second approach may result in reliability and lifetime concerns, such as degradation in the gate oxide integrity and electromigration. To determine the increase in delay, T in (7) is calculated as

$$T = T_{\mathrm{Nominal}} + n\sigma_N \tag{8}$$

where T_{Nominal} is defined as the nominal or mean critical-path delay with no parameter deviations present, n is the required number of standard deviations corresponding to a desired yield, and σ_N is the nominal critical-path delay distribution standard deviation. Computing the increase in power dissipation to guarantee that a specified percentage of critical paths satisfy T_{Nominal}, the supply voltage is increased to shift the nominal distribution as pictured in Fig. 3(a). The nominal distribution is shifted by $n\sigma_T$, where σ_T is the target critical-path delay distribution standard deviation. Fig. 3(b) illustrates the proba

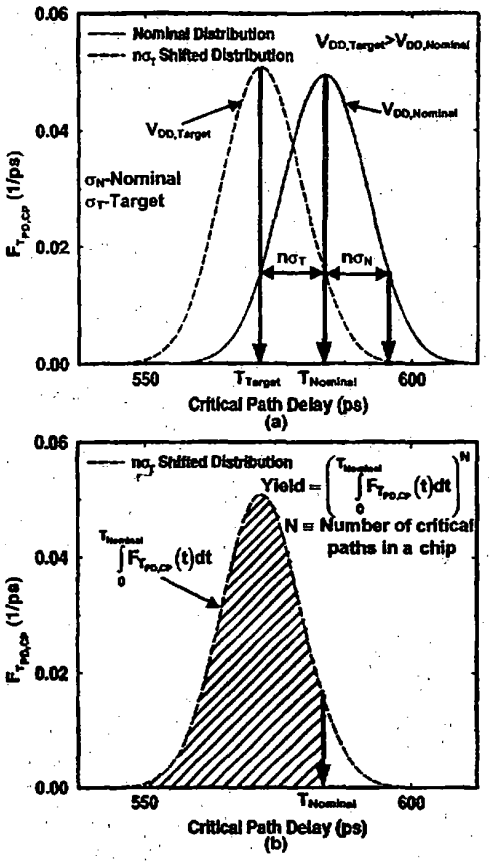

Fig. 3. (a) $n\sigma_T$ critical-path delay distribution shift from the nominal delay (T_{Nominal}) due to an increase in V_{DD} for a (b) desired yield given in (7).

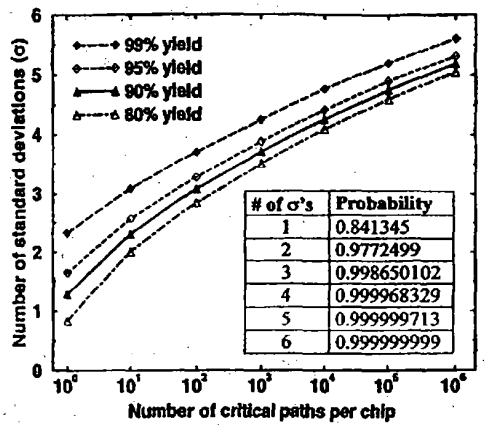

Fig. 4. Number of σ's required to achieve a yield of 80%–99% for a Gaussian distribution versus the number of critical paths on a chip. The table defines the number of σ's and their corresponding probabilities.

TABLE 1
NOMINAL VALUES USED IN ANALYSIS

F (nm)	L (nm)	N_A ($\times 10^{18}$ cm^{-3})	T_{OX} (nm)	V_{DD} (V)	V_T (V)	n_{cp} (#gates)	$P_{Nominal}$ (μW/gate)	$T_{Nominal}$ (ps)
250	200	0.35	4.6	2.21	0.32	15	14.4	1,733
180	144	0.58	3.5	1.81	0.31	12	10.5	1,194
150	120	0.76	2.7	1.48	0.30	12	7.1	1,075
130	104	0.99	2.3	1.33	0.30	10	6.6	787
100	80	1.65	1.8	1.13	0.30	8	5.3	582
70	56	2.56	1.2	0.83	0.26	7	3.1	424
50	40	5.00	0.8	0.66	0.26	5	2.4	283

bility of one critical path having a delay less than or equal to T_{Nominal} as an integration of the target distribution from 0 to T_{Nominal}. This probability raised to the Nth power is the yield. The amount of increase in V_{DD} is determined by calculating the new critical-path target delay

$$T_{\text{Target}} = T_{\text{Nominal}} - n\sigma_T. \tag{9}$$

As the nominal delay distribution is shifted due to an increase in V_{DD}, the deviation of target delay will be reduced such that $\sigma_N > \sigma_T$. Describing the critical-path propagation delay as

$$T_{PD,CP} \propto \frac{V_{DD}}{(V_{DD} - V_T)^{\alpha}} \tag{10}$$

where α is a value between 1 and 2 depending on the amount of velocity saturation [13], the physical reason why $\sigma_N > \sigma_T$ can be explained. As V_{DD} is increased the effect of the threshold voltage (V_T) deviations, due to variations in L, N_A, and T_{OX}, is reduced in $T_{PD,CP}$. Therefore, an iteration process of calculating T_{Target} is required for complete accuracy.

In order to determine n in (8) and (9), Fig. 4 plots the number of standard deviations required to achieve a yield of 80%–99% for a Gaussian distribution versus the number of critical paths per chip. Fig. 4 provides a direct look-up to identify the necessary value of n by coupling the desired yield with the estimated number of critical paths in a chip. The number of critical paths per chip is dependent on the system architecture and optimization procedures, which may vary substantially from one microprocessor design to another. Due to the complicated nature of this issue, determining the number of critical paths for a given technology generation is extremely difficult. Ideally, each transistor would be placed within a critical path to obtain a 100% timing utilization; however, data dependencies as well as other limitations in actual designs restrict the amount of critical-path transistors. Assuming 100–1000 critical paths [10] for today's 10 million transistor microprocessors, a 3σ critical-path delay deviation may be an acceptable tolerance to maintain a reasonable yield as shown in Fig. 4. However, as the number of transistors per chip continues to increase as projected by the roadmap (1.4 billion for the 50-nm generation) [14] and assuming the ratio of critical paths to transistors remains relatively constant, the acceptable tolerance may increase to a 6σ critical-path delay deviation to satisfy future yield requirements, as illustrated in Fig. 4. To cover a range of possible requirements for future technology generations, this paper provides an analysis of the 3σ and 6σ critical-path delay deviations.

The values for feature size (F) and oxide thickness are chosen in the range of parameters projected by the National Technology Roadmap for Semiconductors [14]. Effective channel length is assumed 80% of the feature size [14]. Threshold voltage is calculated by equating the subthreshold drain current [3] per unit width ($V_{GS} = 0$ and $V_{DS} = V_{DD}$) to the maximum off-current per unit width given in the roadmap [14]. The nominal supply voltage is determined by equating the saturation current [3] per

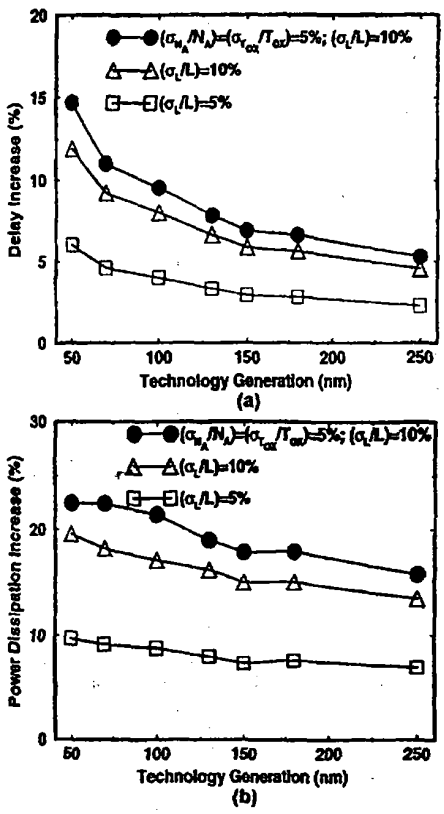

Fig. 5. (a) Delay and (b) power dissipation increases due to extrinsic fluctuations corresponding to a 3σ critical-path delay deviation.

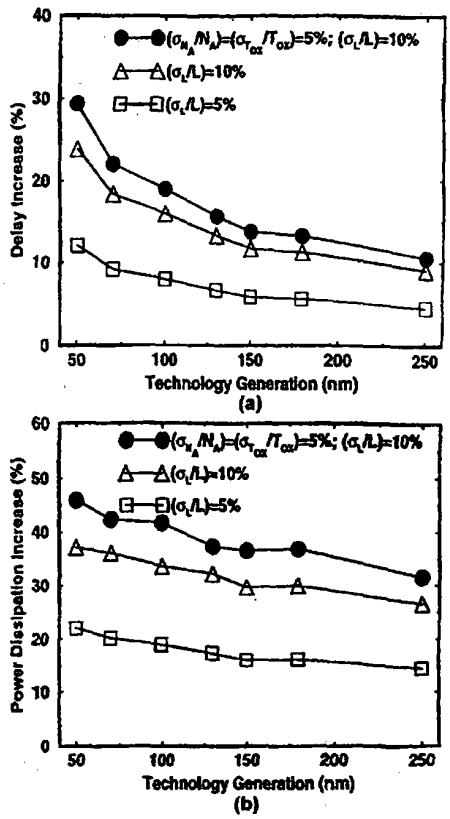

Fig. 6. (a) Delay and (b) power dissipation increases due to extrinsic fluctuations corresponding to a 6σ critical-path delay deviation.

unit width ($V_{GS} = V_{DS} = V_{DD}$) to the nominal on-current per unit width provided in the roadmap [14]. The (W_n/L) ratio is assumed to be 20 [14] and the (W_p/L) ratio is calculated as 23 to obtain equivalent worst case charging and discharging delays for the two-input CMOS NAND gate. Following historical trends [15], the number of gates in the critical path is scaled from 15 to 5 across the 250–50-nm technology generations to enable high performance local clock frequencies. Table I provides the values of $F, L, N_A, T_{OX}, V_{DD}, V_T$, and n_{cp} used for each technology generation analyzed in this paper as well as the calculated nominal values of power dissipation per gate and critical-path delay.

Figs. 5 and 6 illustrate the delay and power dissipation increase due to a range of extrinsic parameter fluctuations in L, N_A, and T_{OX} corresponding to a 3σ and 6σ critical-path delay deviation, respectively. The range of extrinsic parameter fluctuations in L, N_A, and T_{OX} were chosen judiciously in order to provide a useful analysis for today's manufacturing processes (σ_L/L = 5–10%) [14], [16] as well as for future projections ($\sigma_{N_A}/N_A = \sigma_{T_{OX}}/T_{OX}$ = 5%; σ_L/L = 10%). For a 3σ deviation, Fig. 5 indicates a percentage increase in delay and power dissipation ranging from 6% to 15% and 10% to 22%, respectively, for the 50-nm technology generation, depending on the magnitude of device parameter fluctuations. For a 6σ deviation, Fig. 6 demonstrates a percentage increase in delay and power dissipation ranging from 12% to 29% and 22% to 46%, respectively, for the 50-nm technology generation.

The percentage increase in delay and power dissipation grows steadily over the technology generations, which is due to the reduction of the number of gates in the critical path [12] from (5) and (6) according to

$$\frac{\sigma_{T_{PD,CP}}}{\mu_{T_{PD,CP}}} = \frac{\sqrt{n_{cp}}\sigma_{T_{PD,NAND}}}{n_{cp}\mu_{T_{PD,NAND}}} = \frac{1}{\sqrt{n_{cp}}}\frac{\sigma_{T_{PD,NAND}}}{\mu_{T_{PD,NAND}}}. \quad (11)$$

Thus, the ratio of standard deviation to mean for the critical-path delay is inversely proportional to the square root of n_{cp}.

III. Impact of Intrinsic Fluctuations on the Critical Path Delay Distribution

As MOSFET's continue to scale, the fluctuations in the location of dopant atoms in the device active region induce drain-current fluctuations. This is an intrinsic effect since it cannot be eliminated by external control of conventional manufacturing processes. By introducing the "cube model," viewing a MOSFET as an array of MOS capacitors separating the source from the drain, the distribution of dopant atoms is derived from fundamental device analysis [4]. Utilizing the dopant atom distribution, a threshold voltage distribution is derived [4] and compared with experimental data [17] to provide validation for the model calculations, as shown in Fig. 7.

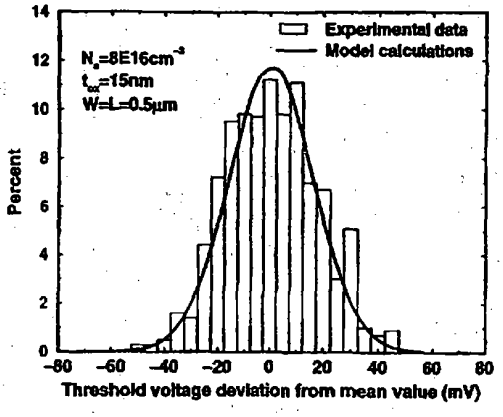

Fig. 7. Comparison of compact model calculated V_T distribution [4] with experimental data [17].

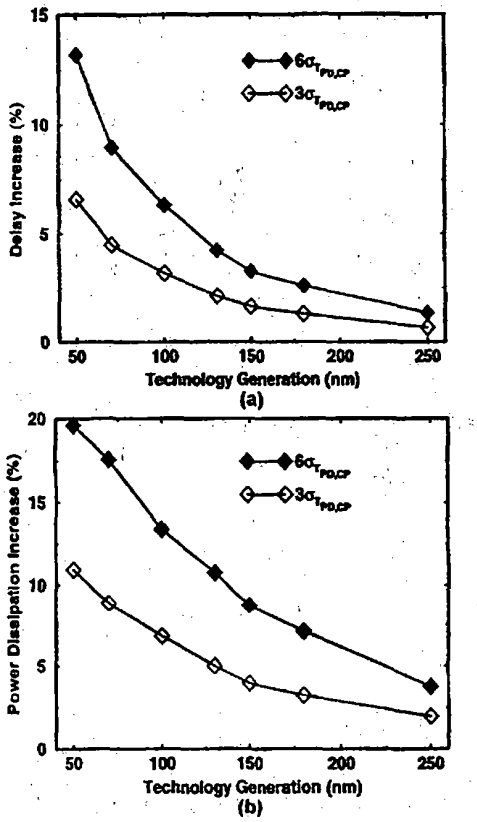

Fig. 8. (a) Delay and (b) power dissipation increases due to intrinsic fluctuations corresponding to a 3σ and 6σ critical-path delay deviation.

The propagation delay distribution density functions for the nFET and pFET are derived as

$$F_{T_{PDn/p}} = \frac{dQ_{n/p}}{dT_{PDn/p}} = F(n_{a/d}) \times \frac{dn_{a/d}}{dT_{PDn/p}} \qquad (12)$$

where $Q_{n/p}$ is the probability that the nFET/pFET propagation delay is less than a specific value, $F(n_{a/d})$ is the effective doping concentration distribution density function for the

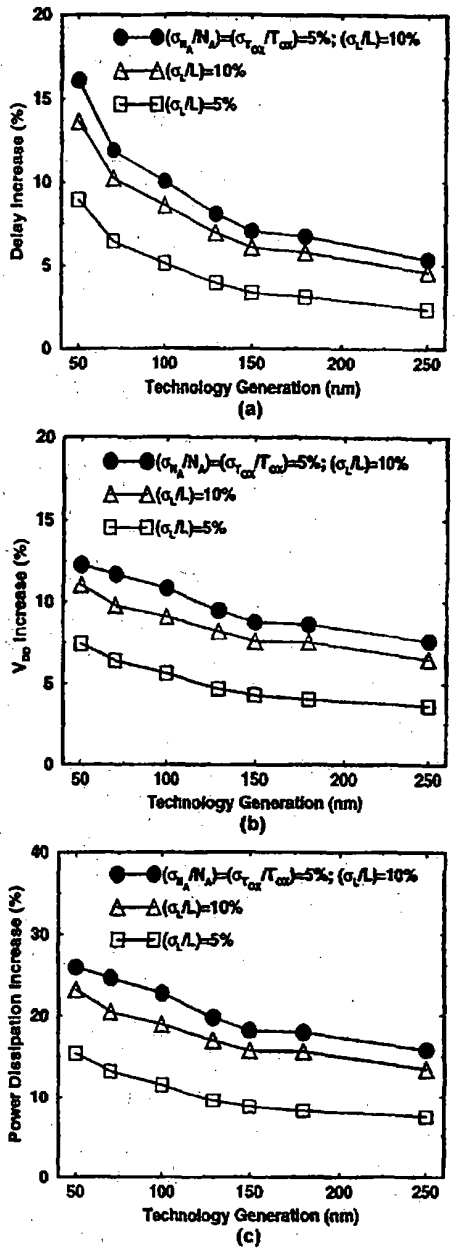

Fig. 9. (a) Delay, (b) supply voltage, and (c) power dissipation increases due to extrinsic and intrinsic fluctuations corresponding to a 3σ critical-path delay deviation.

nFET/pFET [4], and $n_{a/d}$ is the effective doping concentration for the nFET/pFET [4]. The effective doping concentration corresponds to the doping density required for a uniformly doped MOSFET without fluctuations to achieve a specific threshold voltage. The intrinsic deviations are independent from device to device, thus, allowing the NAND gate propagation delay distribution density function due to intrinsic variations to b calculated by (2). Then the critical-path delay distribution is computed as in (4)–(6). Using the same methodology as discussed in Section II for extrinsic variations, the impact of intrinsic fluctuations on

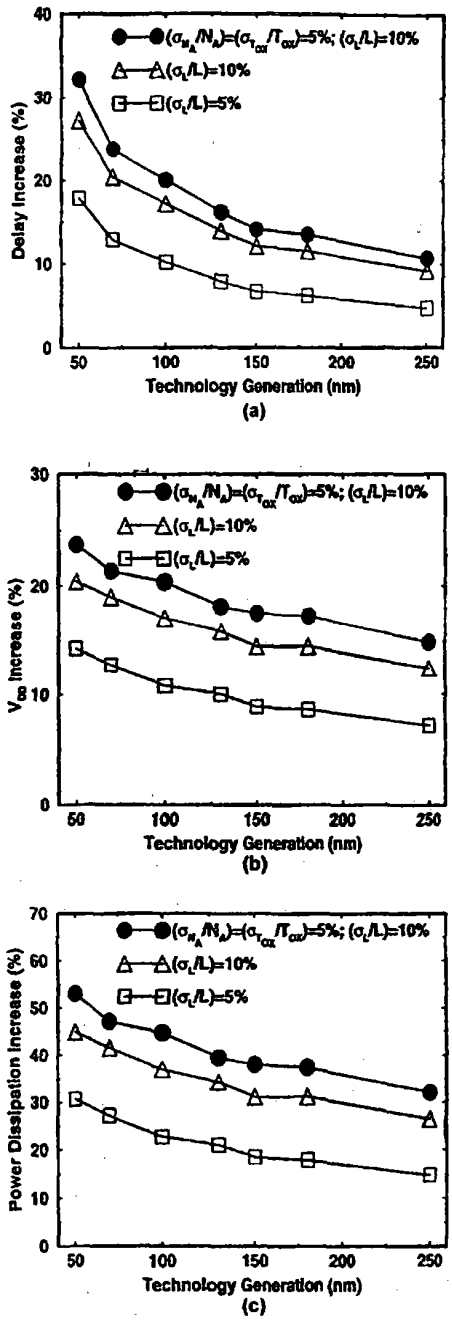

Fig. 10. (a) Delay, (b) supply voltage, and (c) power dissipation increases due to extrinsic and intrinsic fluctuations corresponding to a 6σ critical-path delay deviation.

CMOS circuit performance is examined. Fig. 8 evaluates the delay and power dissipation increases due to intrinsic parameter fluctuations. Fig. 8(a) indicates a percentage increase in delay of 7% and 13%, corresponding to 3σ and 6σ critical-path delay variations respectively, for the 50-nm technology generation. For identical conditions, Fig. 8(b) demonstrates a percentage increase in power dissipation of 11% and 20%.

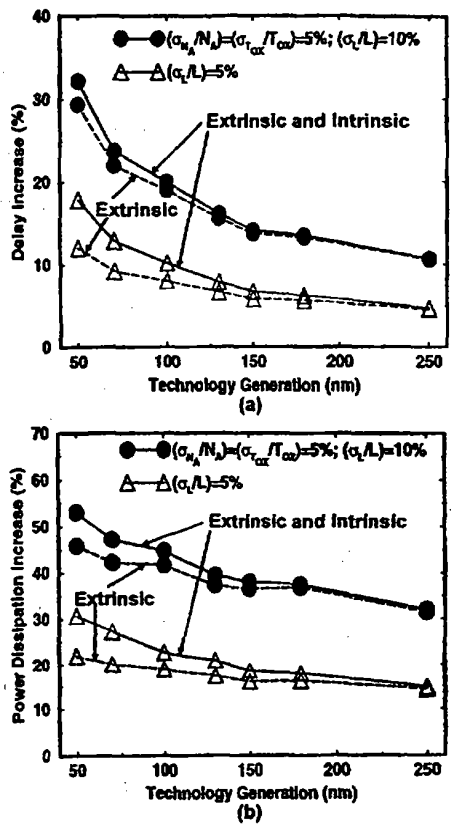

Fig. 11. Impact of including intrinsic fluctuations on (a) delay and (b) power dissipation corresponding to a 6σ critical-path delay deviation.

IV. Impact of Both Extrinsic and Intrinsic Fluctuations on the Critical Path Delay Distribution

In the previous two sections, the impact of extrinsic and intrinsic fluctuations on CMOS circuit performance was demonstrated individually, now the extrinsic and intrinsic parameter fluctuations will be combined. Assuming the extrinsic and intrinsic fluctuations are independent, the combined effect on the NAND gate delay distribution is calculated [11] as

$$\sigma_{T_{PD,\mathrm{NAND}}} = \sqrt{\sigma^2_{T_{PD,\mathrm{NAND-EXT}}} + \sigma^2_{T_{PD,\mathrm{NAND-INT}}}} \qquad (13)$$

where $\sigma_{T_{PD,\mathrm{NAND-EXT}}}$ and $\sigma_{T_{PD,\mathrm{NAND,INT}}}$ are the standard deviations due to extrinsic and intrinsic variations respectively. Now the critical-path delay distribution is calculated as in (4)–(6) for both extrinsic and intrinsic fluctuations.

Figs. 9 and 10 quantify the delay, supply voltage, and, resulting power dissipation increases due to both extrinsic and intrinsic parameter fluctuations corresponding to 3σ and 6σ critical-path delay deviations, respectively. For a 3σ deviation, Fig. 9 exhibits a percentage increase in delay, supply voltage, and power dissipation ranging from 9% to 16%, 7% to 12%, and 15% to 26%, respectively, for the 50-nm technology generation, depending on the magnitude of extrinsic parameter fluctuations. For a 6σ deviation, Fig. 10 projects significant percentage increases in delay, supply voltage, and power

dissipation ranging from 18% to 32%, 14% to 24%, and 31% to 53%, respectively, for the 50-nm technology generation. Comparing Fig. 6 (extrinsic fluctuations only) with Fig. 10 (extrinsic and intrinsic fluctuations) for the 50-nm technology generation, Fig. 11 indicates that the impact of intrinsic fluctuations increases the delay from 12%–29% to 18%–32% and power dissipation from 22%–46% to 31%–53%, depending on the magnitude of extrinsic fluctuations, corresponding to the 6σ critical-path delay deviation.

V. Conclusion

A static CMOS critical-path delay distribution due to extrinsic macroscopic manufacturing process fluctuations and intrinsic microscopic random dopant fluctuations is developed and analyzed. Two possible options for achieving a desired yield are explored: 1) reduce performance by operating at a lower clock frequency; and 2) increase the supply voltage and, consequently, power dissipation, to satisfy the nominal critical-path delay. For the 50-nm technology generation, the delay and power dissipation increases due to extrinsic fluctuations only are calculated as 12%–29% and 22%–46%, respectively, for extrinsic parameter standard deviations ranging from 5% for effective channel length and 0% for gate oxide thickness and channel doping concentration to 10% for effective channel length and 5% for gate oxide thickness and channel doping concentration. In comparison, when both extrinsic and intrinsic fluctuations are included in the analysis, the delay and power dissipation increases to 18%–32% and 31%–53%, respectively, thus demonstrating the importance of incorporating intrinsic fluctuations into future CMOS logic circuit designs.

Acknowledgment

The authors wish to thank Avant! Corporation for their support of the TCAD tools.

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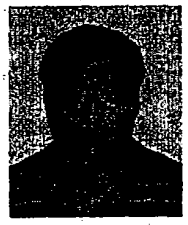

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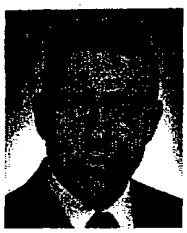
Dr. Eble received the Best Paper Award at the 1997 International ASIC Conference.



James D. Meindl (M'56–SM'66–F'68–LF'97) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1955, 1956, and 1958, respectively.

He is currently the Director of the Joseph M. Pettit Microelectronics Research Center and the Pettit Chair Professor of Microelectronics, Georgia Institute of Technology, Atlanta. Previously he served from 1986 to 1993 as Senior Vice President for Academic Affairs and Provost of Rensselaer Polytechnic Institute, Troy, NY. From 1967 through 1986 he was with Stanford University, Stanford, CA, where he was the John M. Fluke Professor of Electrical Engineering, Associate Dean for Research in the School of Engineering, Director of the Center for Integrated Systems, Director of the Electronics Laboratories, and founding Director of the Integrated Circuits Laboratory. He is a co-founder of Telesensory Systems, Inc., the principal manufacturer of electronic reading aids for the blind, and he served as a Member of the Board from 1971 through 1984. From 1965 through 1967 he was founding Director of the Integrated Electronics Division, U.S. Army Electronics Laboratories, Fort Monmouth, NJ. He is the author of the book *Micropower Circuits* and over 500 technical papers on ultra large scale integration, integrated electronics, and medical electronics. He is the editor of the book *Brief Lessons in High Technology*, which elucidates the most important economic event of our lives, the emergence of the information society. His major contributions have been new medical instruments enabled by custom integrated electronics, projections and codification of the hierarchy of physical limits on integrated electronics, and leadership in creation of academic environments promoting high quality teaching and research.

Dr. Meindl is a Life Fellow of the American Association for the Advancement of Science, and a member of the American Academy of Arts and Sciences and the National Academy of Engineering and its Academic Advisory Board. Dr. Meindl received the IEEE Third Millennium Medal, the 1999 SIA University Research Award, the 1997 Hamerschlag Distinguished Alumnus Award from Carnegie Mellon University, and the 1991 Benjamin Garver Lamme Medal from ASEE. He was the recipient of the 1990 IEEE Education Medal "for establishment of a pioneering academic program for the fabrication and application of integrated circuits" and the recipient of the 1989 IEEE Solid-State Circuits Medal for contributions to solid-state circuits and solid-state circuit technology. At the 1988 IEEE International Solid-State Circuits Conference, he received the Beatrice K. Winner Award. In 1980 he was the recipient of the IEEE Electron Devices Society's J.J. Ebers Award for his contributions to the field of medical electronics and for his research and teaching in solid-state electronics. From 1970 through 1978 Dr. Meindl and his students received five outstanding paper awards at IEEE International Solid-State Circuits Conferences, along with one received at the 1985 IEEE VLSI Multilevel Interconnections Conference.

DOCKET NO: 282-I0217
SERIAL NO:
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